

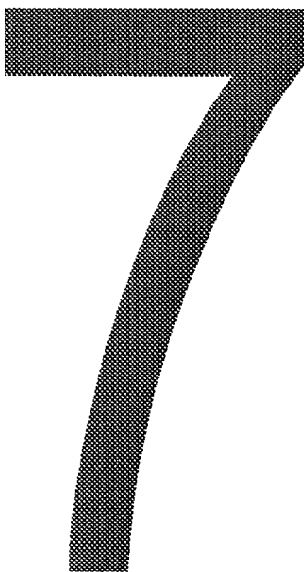
### Abstract

In order to enable high speed, high bandwidth data transfer between two ASIC devices, for example in a backplane, a wide parallel input data word is divided into a smaller number of words, and each smaller word is converted to serial form and then  
5 transmitted over a respective sub-link at a high clock rate relative to the system clock. At the receiving side, the clock is recovered from the serial words, and the serial words are converted back to parallel form. An alignment process is then carried out, firstly involving detecting the positions of the bits of the words and then storing the words in a buffer FIFO register. The words are clocked out of the FIFO register in synchronism  
10 under control of the system clock once it is detected that valid words are received in the FIFO registers.

UNITED STATES PATENT AND TRADEMARK OFFICE  
DOCUMENT CLASSIFICATION BARCODE SHEET



# Drawings



Level - 2  
Version 1.1

FIG. 1

Link Interface Transmit

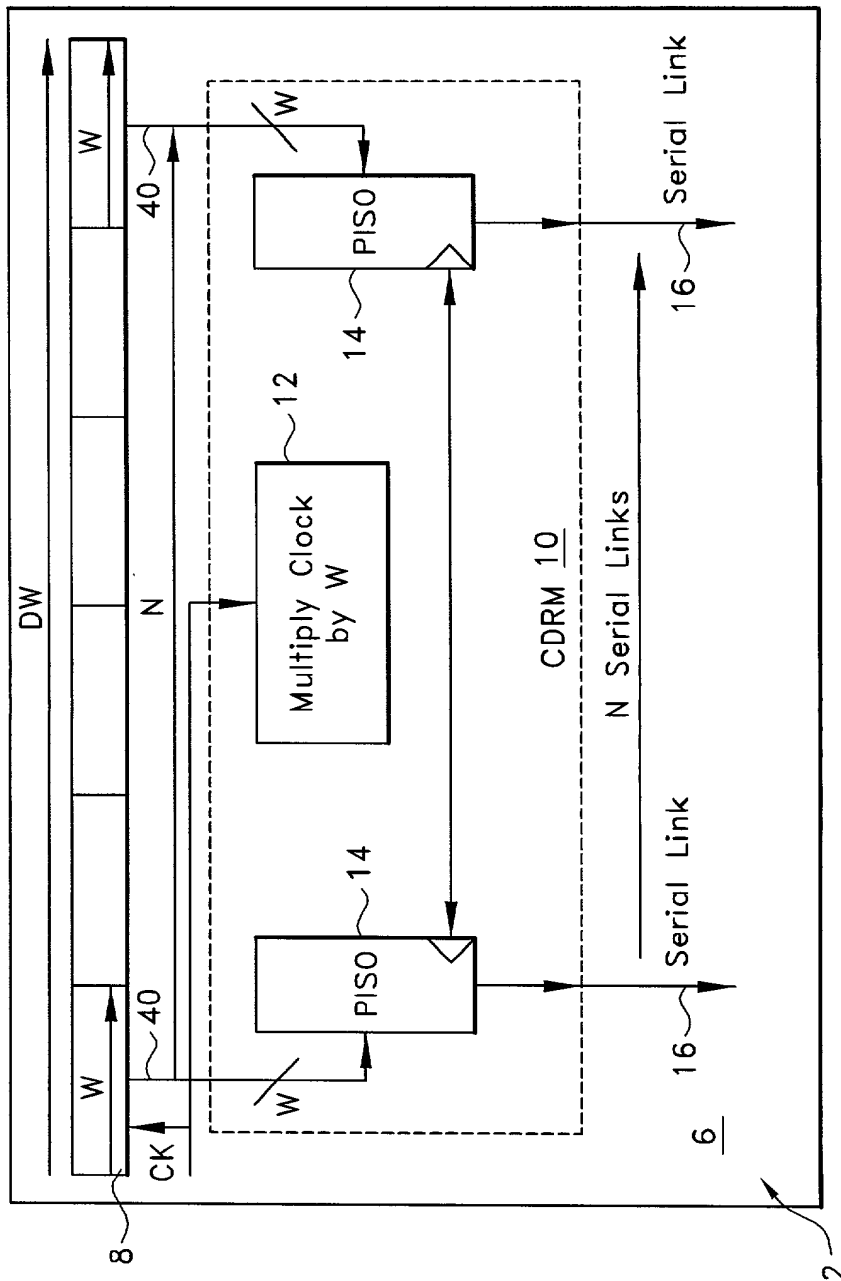
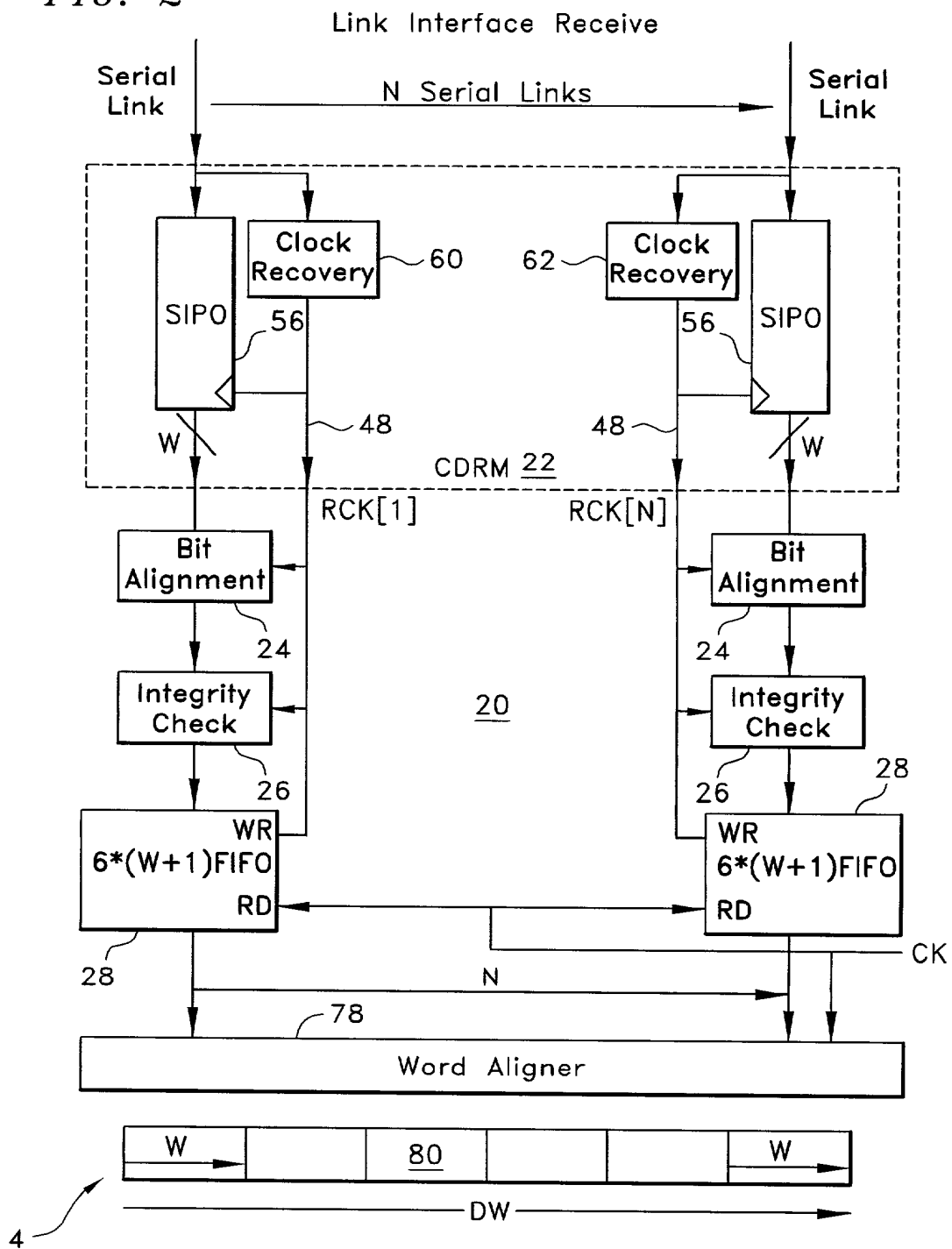


FIG. 2



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FIG. 3

## Word Aligner Trigger

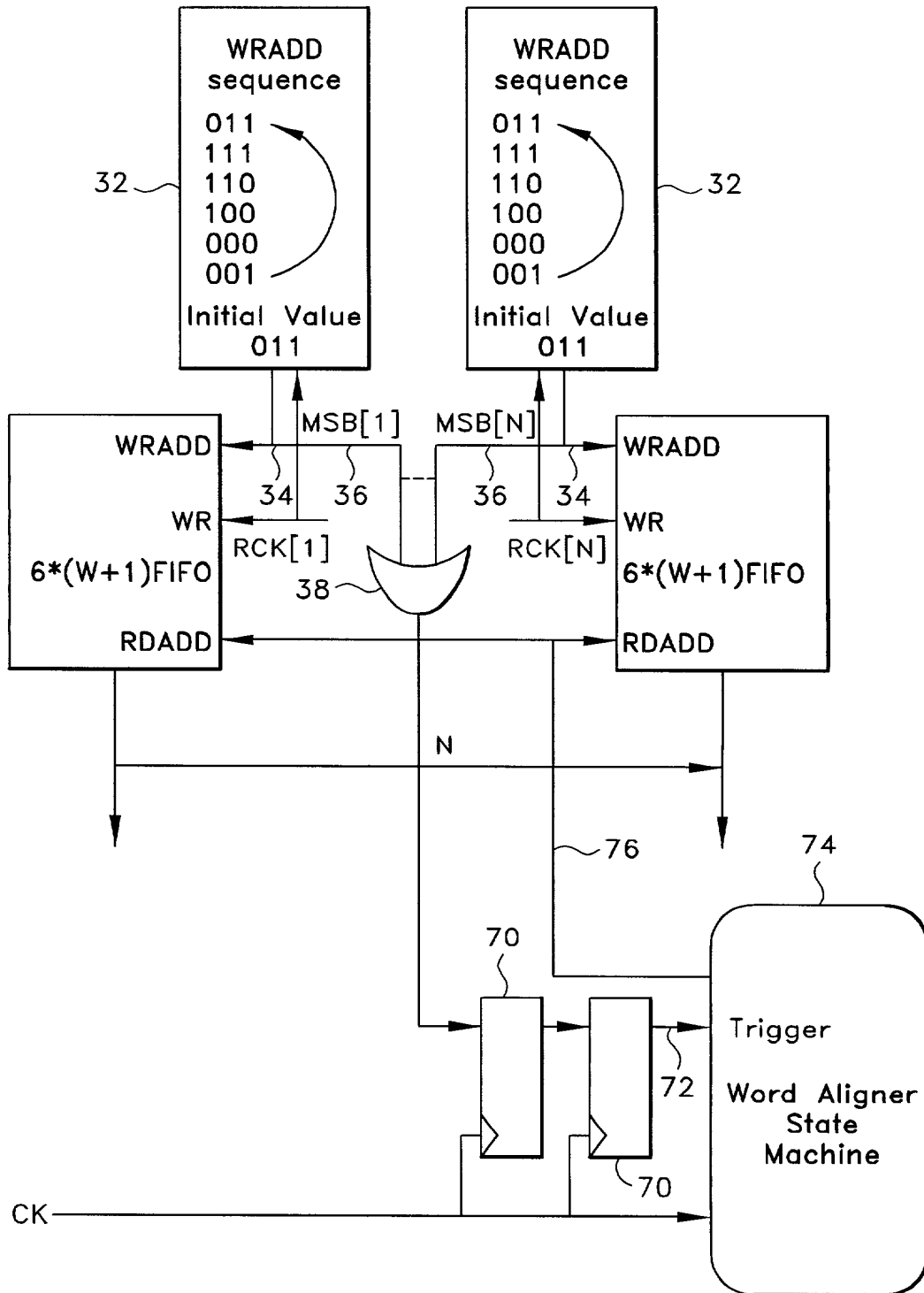


FIG. 4

## Clock Data Recovery Module

